

*bd*RDI

JTAG debug interface for RDI compatible debuggers

ARM / ARM9



User Manual

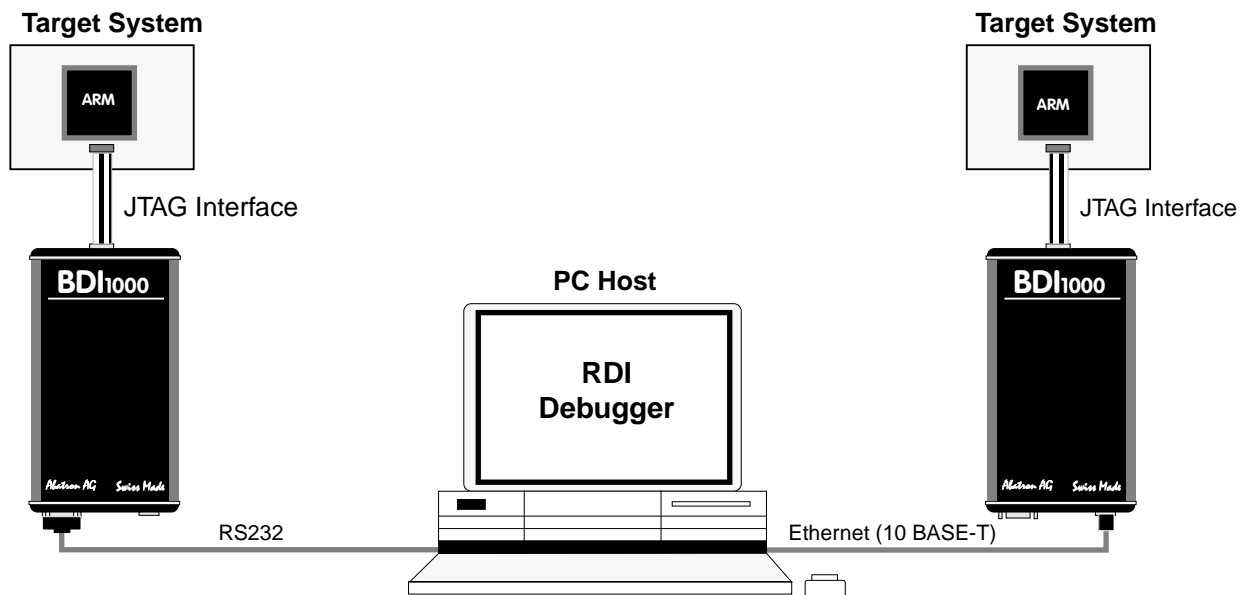
Manual Version 1.12 for BDI1000



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1 Introduction



The BDI1000 adds JTAG based debugging to RDI compatible debuggers (e.g. ADW from ARM Ltd). With the BDI1000, you control and monitor the microcontroller solely through the stable on-chip debugging services. You won't waste time and target resources with a software ROM monitor, and you eliminate the cabling problems typical of ICE's. This combination runs even when the target system crashes and allows developers to continue investigating the cause of the crash. A RS232 interface with a maximum of 115 kBaud and a 10Base-T Ethernet interface is available for the host interface. The configuration software is used to update the firmware and to configure the BDI1000 so it works with the RDI compatible debugger.

1.1 BDI1000

The BDI1000 is a processor system in a small box. It implements the interface between the JTAG pins of the target CPU and a 10Base-T Ethernet / RS232 connector. The firmware and the programmable logic of the BDI1000 can be updated by the user with a simple Windows based configuration program. The BDI1000 supports target system voltages from 1.8 up to 5 Volts.

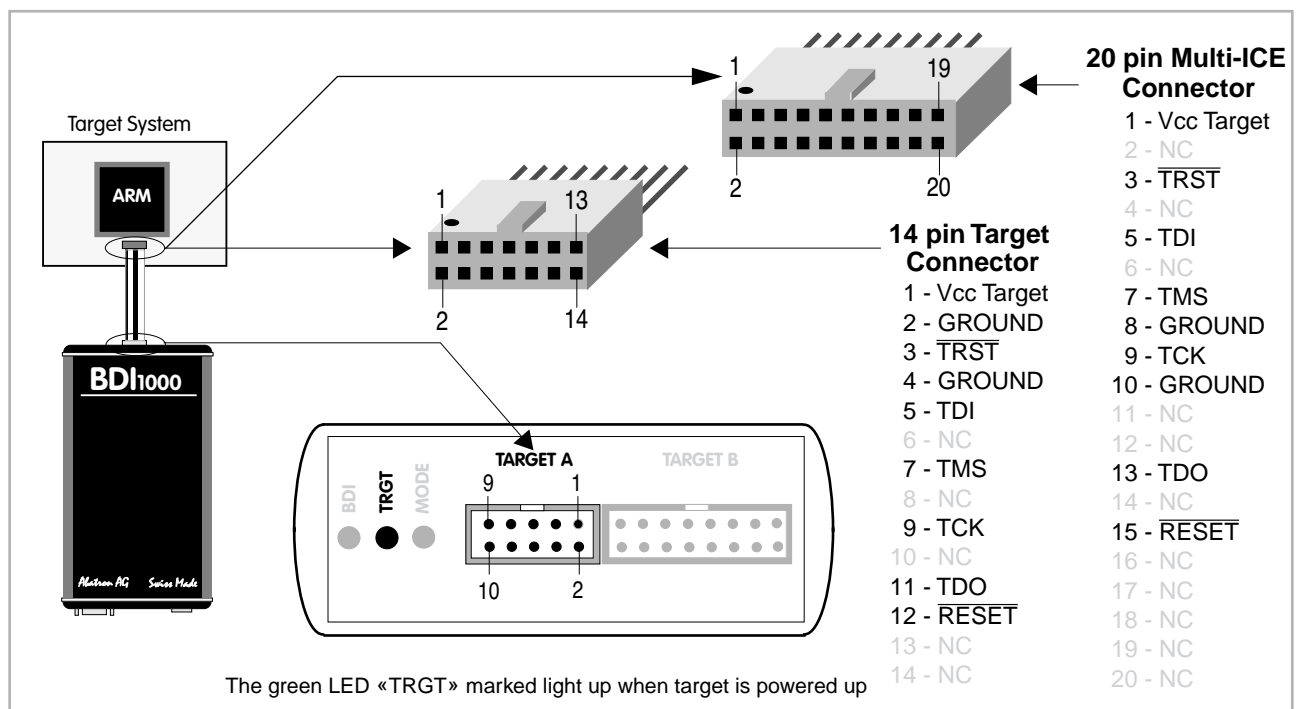
2 Installation

2.1 Connecting the BDI1000 to Target

The enclosed cables to the target system are designed for the ARM Development Boards. In case where the target system has the same connector layout, the cable (14 pin or 20 pin) can be directly connected.



In order to ensure reliable operation of the BDI (EMC, runtimes, etc.) the target cable length must not exceed 20 cm (8").



TARGET A connector signals see table on next page.

TARGET A Connector Signals

Pin	Name	Description
1	reserved	This pin is currently not used.
2	$\overline{\text{TRST}}$	JTAG Test Reset This open-drain / push-pull output of the BDI1000 resets the JTAG TAP controller on the target. Default driver type is open-drain.
3+5	GND	System Ground
4	TCK	JTAG Test Clock This output of the BDI1000 connects to the target TCK line.
6	TMS	JTAG Test Mode Select This output of the BDI1000 connects to the target TMS line.
7	$\overline{\text{RESET}}$	This open collector output of the BDI1000 is used to reset the target system.
8	TDI	JTAG Test Data In This output of the BDI1000 connects to the target TDI line.
9	Vcc Target	1.8 – 5.0V: This is the target reference voltage. It indicates that the target has power and it is also used to create the logic-level reference for the input comparators. It also controls the output logic levels to the target. It is normally connected to Vdd I/O on the target board.
10	TDO	JTAG Test Data Out This input to the BDI1000 connects to the target TDO line.

The BDI1000 works also with targets which have no dedicated $\overline{\text{TRST}}$ pin. For this kind of targets, the BDI cannot force the target to debug mode immediately after reset. The target always begins execution of application code until the BDI has finished programming the Debug Control Register.

2.1.1 Changing Target Processor Type

Before you can use the BDI1000 with an other target processor type (e.g. ARM <--> PPC), a new setup has to be done (see chapter 2.6 «Configuration»). During this process the target cable must be disconnected from the target system. The BDI1000 needs to be supplied **between 2.5V and 5V** via the POWER connector. For more information see chapter 2.2.1 «External Power Supply».



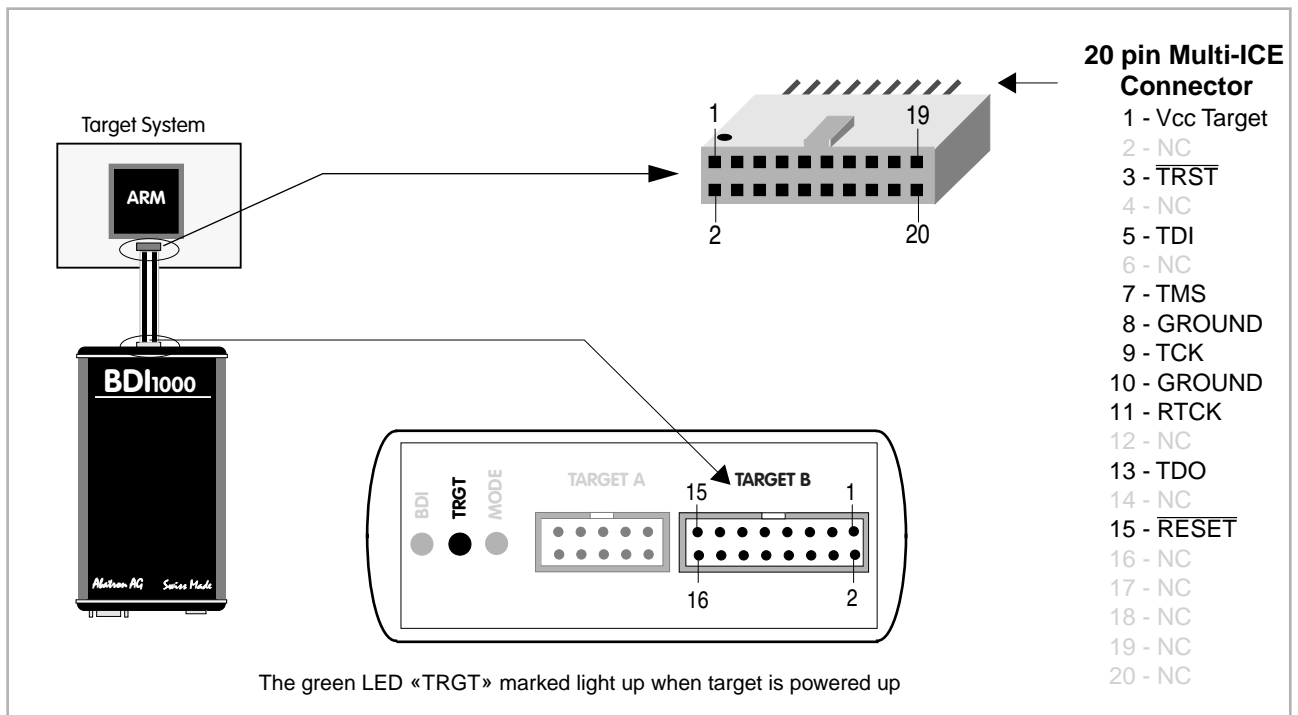
To avoid data line conflicts, the BDI1000 must be disconnected from the target system while programming the logic for an other target CPU.

2.1.2 Adaptive Clocking

Adaptive clocking is a feature which ensures that the BDI1000 never loses synchronization with the target device, whatever the target clock speed is. To achieve this, BDI1000 uses two signals TCK and RTCK. When adaptive clocking is selected, BDI1000 issues a TCK signal and waits for the Returned TCK (RTCK) to come back. BDI1000 does not progress to the next TCK until RTCK is received. For more information about adaptive clocking see ARM documentation.

Note:

Adaptive clocking is only supported with a special target cable. This special cable can be ordered separately from Abatron.



For TARGET B connector signals see table on next page.

BDI TARGET B Connector Signals:

Pin	Name	Description
1	TDO	JTAG Test Data Out This input to the BDI1000 connects to the target TDO line.
2	reserved	
3	TDI	JTAG Test Data In This output of the BDI1000 connects to the target TDI line.
4	reserved	
5	RTCK	Returned JTAG Test Clock This input to the BDI1000 connects to the target RTCK line.
6	Vcc Target	1.8 – 5.0V: This is the target reference voltage. It indicates that the target has power and it is also used to create the logic-level reference for the input comparators. It also controls the output logic levels to the target. It is normally connected to Vdd I/O on the target board.
7	TCK	JTAG Test Clock This output of the BDI1000 connects to the target TCK line.
8	$\overline{\text{TRST}}$	JTAG Test Reset This open-drain / push-pull output of the BDI1000 resets the JTAG TAP controller on the target. Default driver type is open-drain.
9	TMS	JTAG Test Mode Select This output of the BDI1000 connects to the target TMS line.
10	reserved	
11	reserved	
12	GROUND	System Ground
13	$\overline{\text{RESET}}$	System Reset This open collector output of the BDI1000 is used to reset the target system.
14	reseved	
15	reseved	
16	GROUND	System Ground

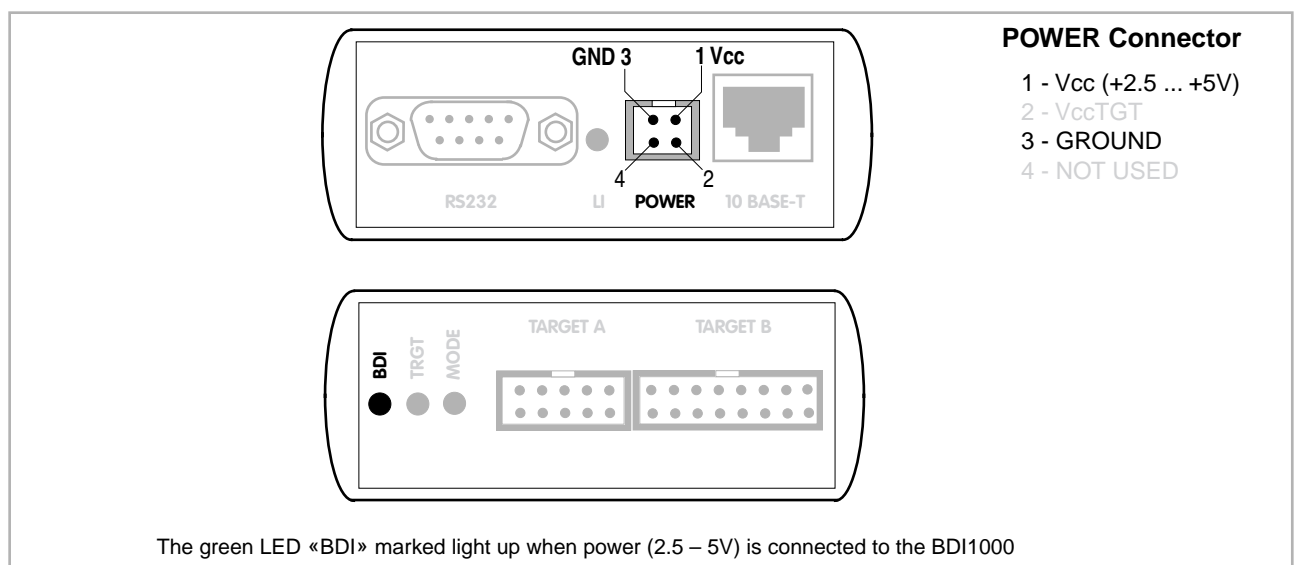
2.2 Connecting the BDI1000 to Power Supply

2.2.1 External Power Supply

The BDI1000 needs to be supplied **between 2.5V and 5V** via the POWER connector. The available power supply from Abatron (option) or the enclosed power cable can be directly connected. In order to ensure reliable operation of the BDI1000, keep the power supply cable as short as possible.



For error-free operation, the power supply to the BDI1000 must be between 2.5V and 5V DC. **The maximal tolerable supply voltage is 5.25 VDC. Any higher voltage or a wrong polarity might destroy the electronics.**



Please switch on the system in the following sequence:

- 1 --> external power supply
- 2 --> target system

2.2.2 Power Supply from Target System

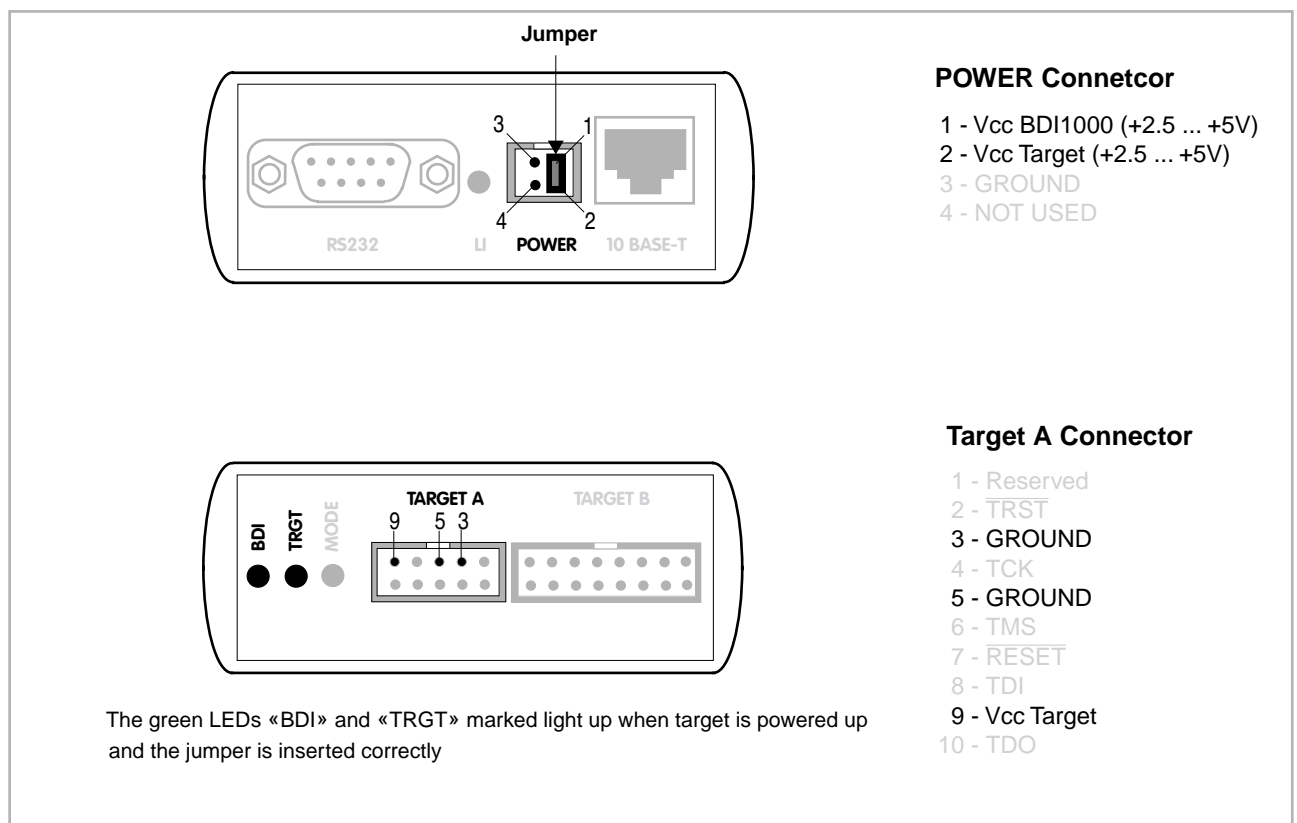
The BDI1000 needs to be supplied between 2.5V and 5V via TARGET A connector. This mode can only be used when the target system runs **between 2.5V and 5V** and the pin «Vcc Target» is able to deliver a current up to:

- 900mA@2.5Vcc Target
- 700mA@3.3Vcc Target
- 450mA@5.0Vcc Target

For pin description and layout see chapter 2.1 «Connecting the BDI1000 to Target». Insert the enclosed Jumper as shown in figure below. **Please ensure that the jumper is inserted correctly.**

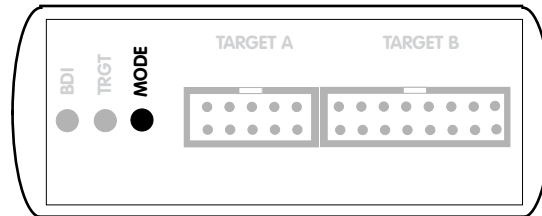


For error-free operation, the power supply to the BDI1000 must be between 2.5V and 5V DC. **The maximal tolerable supply voltage is 5.25 VDC. Any higher voltage or a wrong polarity might destroy the electronics.**



2.3 Status LED «MODE»

The built in LED indicates the following BDI states:

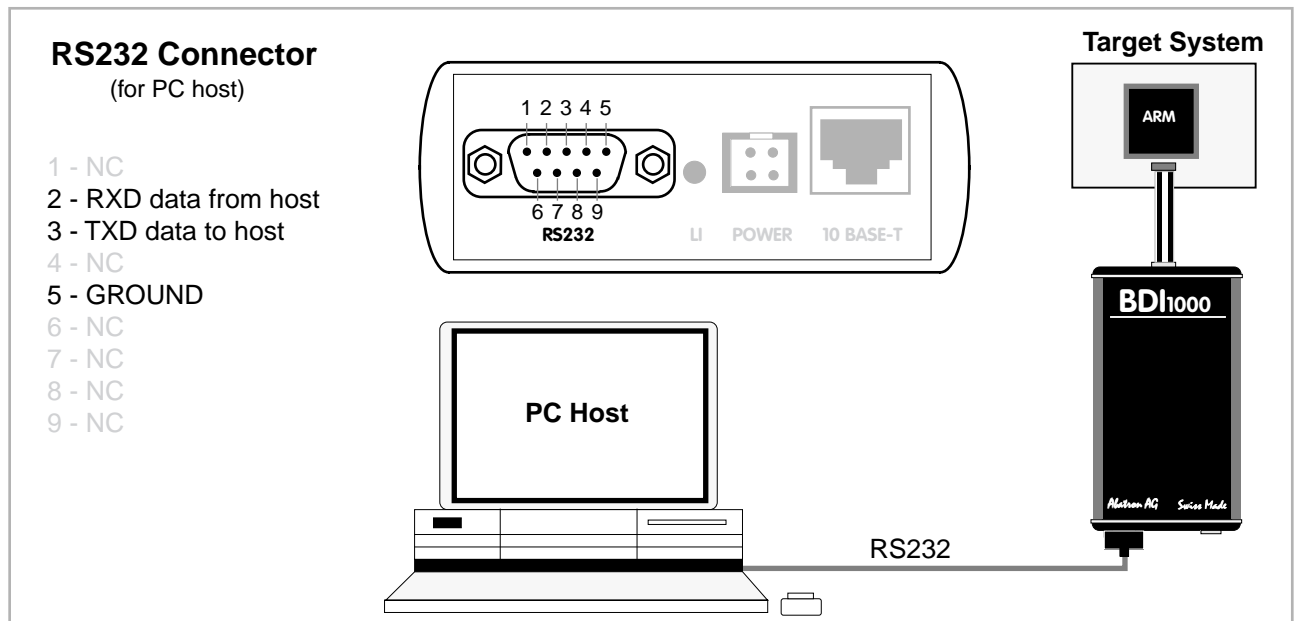


MODE LED	BDI STATES
OFF	The BDI is ready for use, the firmware is already loaded.
ON	The power supply for the BDI1000 is < 2.5VDC.
BLINK	The BDI «loader mode» is active (an invalid firmware is loaded or loading firmware is active).

2.4 Connecting the BDI1000 to Host

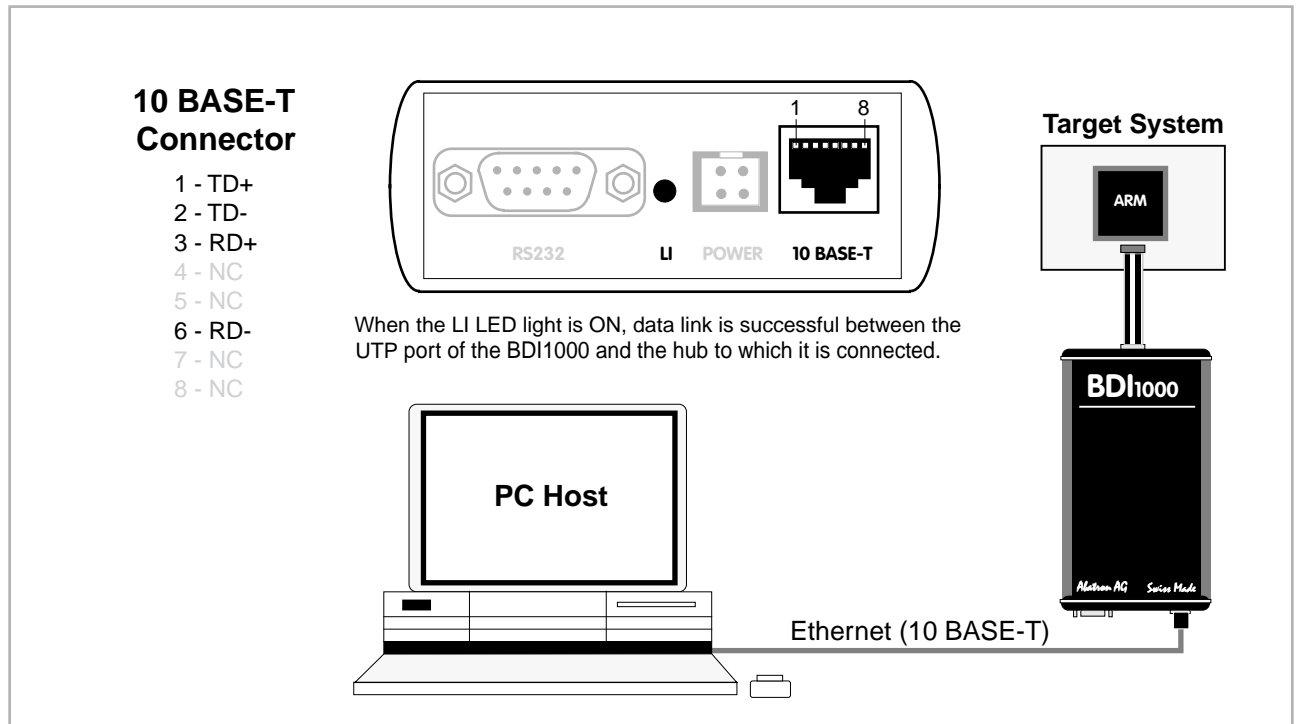
2.4.1 Serial line communication

The host is connected to the BDI through the serial interface (COM1...COM4). The communication cable between BDI and Host is a serial cable (RXD / TXD are crossed). There is the same connector pinout for the BDI and for the Host side (Refer to Figure below).



2.4.2 Ethernet communication

The BDI1000 has a built-in 10 BASE-T Ethernet interface (see figure below). Connect an UTP (Unshielded Twisted Pair) cable to the BD1000. For thin Ethernet coaxial networks you can connect a commercially available media converter (BNC --> 10 BASE-T) between your network and the BDI1000. Contact your network administrator if you have questions about the network.



2.5 Installation of the Configuration Software

On the enclosed diskette you will find the BDI configuration software and the firmware required for the BDI. Copy all these files to a directory on your hard disk.

The following files are on the diskette:

b10arm.exe	Configuration program
b10arm.hlp	Helpfile for the configuration program
b10arm.cnt	Help contents file
b10armfw.xxx	Firmware for BDI1000 for ARM targets
armjed10.xxx	JEDEC file for the BDI logic device programming
bdiifc32.dll	BDI Interface DLL for configuration program
bdiridi.dll	RDI Interface DLL
*.bdi	Configuration Examples

Example of an installation process:

- Copy the entire contents of the enclosed diskette into a directory on the hard disk.
- You may create a new shortcut to the b10arm.exe configuration program.
- The RDI interface DLL has to copied to the appropriate debugger directory

2.6 Configuration

Before you can use the BDI together with the debugger, the BDI must be configured. Use the *SETUP* menu and follow the steps listed below:

- Load or update the firmware / logic, store IP address --> *Firmware*
- Set the communication parameters between Host and BDI --> *Communication*
- Setup an initialization list for the target processor --> *Initlist*
- Select the working mode --> *Mode*
- Transmit the configuration to the BDI --> *Mode Transmit*

For information about the dialogs and menus use the help system (F1).

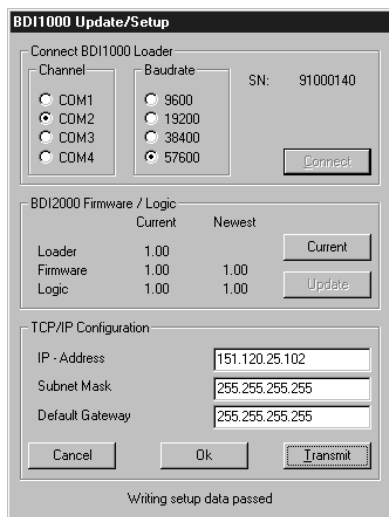
2.6.1 BDI1000 Setup/Update

First make sure that the BDI is properly connected (see Chapter 2.1 to 2.4). The BDI must be connected via RS232 to the Windows host.



To avoid data line conflicts, the BDI1000 must be disconnected from the target system while programming the logic for an other target CPU (see Chapter 2.1.1).

The following dialogbox is used to check or update the BDI firmware and logic and to set the network parameters.



dialog box «BDI1000 Update/Setup»

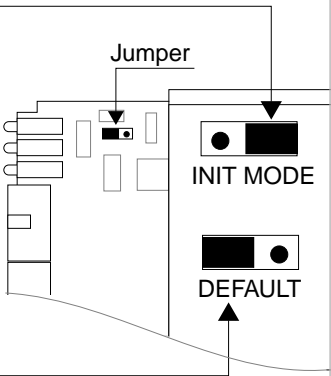
The following options allow you to check or update the BDI firmware and logic and to set the network parameters:

- Channel** Select the communication port where the BDI1000 is connected during this setup session.
- Baudrate** Select the baudrate used to communicate with the BDI1000 loader during this setup session.

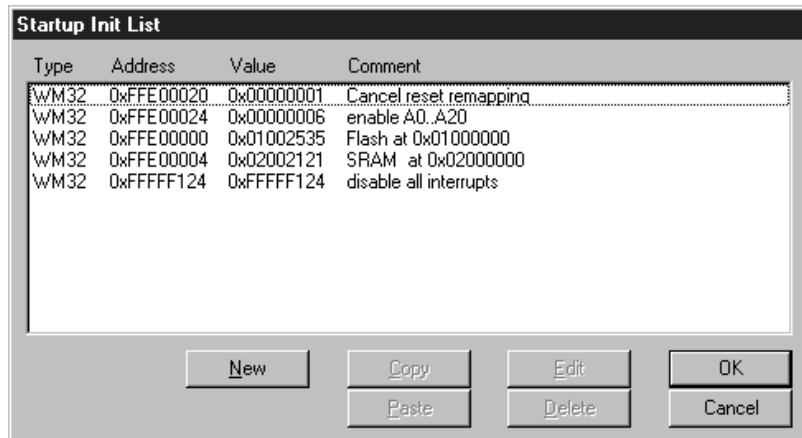
Connect	Click on this button to establish a connection with the BDI1000 loader. Once connected, the BDI1000 remains in loader mode until it is restarted or this dialog box is closed.
Current	Press this button to read back the current loaded BDI1000 software and logic versions. The current loader, firmware and logic version will be displayed.
Update	This button is only active if there is a newer firmware or logic version present in the execution directory of the BDI setup software. Press this button to write the new firmware and/or logic into the BDI1000 flash memory / programmable logic.
IP Address	Enter the IP address for the BDI1000. Use the following format: xxx.xxx.xxx.xx.e.g.151.120.25.101 Ask your network administrator for assigning an IP address to this BDI1000. Every BDI1000 in your network needs a different IP address.
Subnet Mask	Enter the subnet mask of the network where the BDI is connected to. Use the following format: xxx.xxx.xxx.xx.e.g.255.255.255.0 A subnet mask of 255.255.255.255 disables the gateway feature. Ask your network administrator for the correct subnet mask.
Default Gateway	Enter the IP address of the default gateway. Ask your network administrator for the correct gateway IP address. If the gateway feature is disabled, you may enter 255.255.255.255 or any other value..
Transmit	Click on this button to store the network configuration in the BDI1000 flash memory.

In rare instances you may not be able to load the firmware in spite of a correctly connected BDI (error of the previous firmware in the flash memory). **Before carrying out the following procedure, check the possibilities in Appendix «Troubleshooting».** In case you do not have any success with the tips there, do the following:

- Switch OFF the power supply for the BDI and open the unit as described in Appendix «Maintenance»
- Place the jumper in the «**INIT MODE**» position
- Connect the power cable or target cable if the BDI is powered from target system
- Switch ON the power supply for the BDI again and wait until the LED «MODE» blinks fast
- Turn the power supply OFF again
- Return the jumper to the «**DEFAULT**» position
- Reassemble the unit as described in Appendix «Maintenance»



3 Init List



dialog box «Startup Init List»

In order to prepare the target for debugging, you can define an Initialization List. This list is stored in the Flash memory of the BDI1000 and worked through every time the target comes out of reset. Use it to get the target operational after a reset. The memory system is usually initialized through this list. After processing the init list, the RAM used to download the application must be accessible.

Use on-line help (F1) and the supplied configuration examples on the distribution disk to get more information about the init list.

Special BDI Configuration Registers:

In order to change some special configuration parameters of the BDI, the GPR entry in the init list is used. Normal ARM GPR's covers a range from 0 to 15. Other GPR's are used to set BDI internal registers:

8005 This entry in the init list allows to change the JTAG clock frequency. This is useful if you have to start with a slow JTAG clock out of reset but after some initialization (e.g. PLL setup) you can use a faster clock. As an example see AT91EB55 setup. The value you enter selects the following JTAG frequency:

0 = adaptive	5 = 200 kHz
1 = 6 MHz	6 = 100 kHz
2 = 3 MHz	7 = 50 kHz
3 = 1 MHz	8 = 20 kHz
4 = 500 kHz	9 = 10 kHz

8006 This entry in the init list allows to define a delay time (in ms) the BDI inserts between releasing the reset line and starting communicating with the target. This delay is necessary when a target needs some wake-up time after a reset (e.g. Cirrus EP7209).

8007 By default, the BDI asserts the RESET signal during reset processing. After writing zero to this special register, the BDI no longer drives RESET low. This may be useful in some special cases.

8008 During JTAG debugging, the PC increments while the BDI stuffs instruction into the ARM core. It may be necessary to set the PC to a safe non-vector address before external memory is accessed to prevent pre-fetching code from an invalid address range. Enter a safe non-vector address for the PC into this special BDI registers..

8009 By default, the TRST signal is driven with an open-drain driver by the BDI. Write a 1 to this special BDI register if the TRST signal should be driven with a push-pull driver.

8010 By default, on ARM7 based targets the BDI uses a software breakpoint to support semi hosting. In cases where the vector table is allocated to ROM, write a 1 to this special BDI registers to force the use of a hardware breakpoint. This does not apply to ARM9 targets because on ARM9 there exists a special vector catch feature.

8012 This entry in the init list allows to define a time (in ms) the BDI asserts the hardware reset signal. By default the reset signal is asserted for about 3 ms.

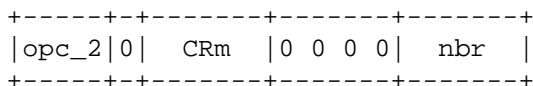
8013 With this entry the MAC7100 "JTAG lockout recovery" can be activated. As value enter the correct CMF clock divider (CMFCLKD). Calculate this value based on the reset frequency, the frequency that is active before any init list entry is processed (PLL is not active). If for example the system clock is 8 MHz, the clock input to the flash is 4MHz and the correct value for CFMCKLD is 19 (0x13). If this entry is present, the BDI automatically recovers a secured flash as part of the next reset sequence.

3.1 Init CP15 Registers

Via the Initialization List it is possible to setup the Coprocessor 15 (CP15) registers. The address part of a WCP15 init list entry uses a special format which depends on the used CPU type.

ARM710T, ARM720T, ARM740T:

The 16bit register number is used to build the appropriate MCR/MRC instruction to access the CP15 register.



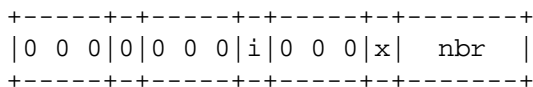
Normally opc_2 and CRm are zero and therefore you can simply enter the CP15 register number.

```
WCP15 0x0002      0x00004000 MMU: set Translation Base Address
```

ARM920T:

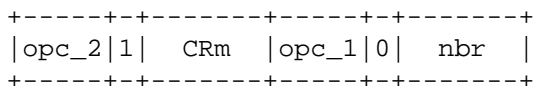
Via JTAG, CP15 registers are accessed either direct (physical access mode) or via interpreted MCR/MRC instructions. Read also ARM920T manual, part "Debug Support - Scan Chain 15".

Register number for physical access mode (bit 12 = 0):



The bit "i" selects the instruction cache (scan chain bit 33), the bit "x" extends access to register 15 (scan chain bit 38).

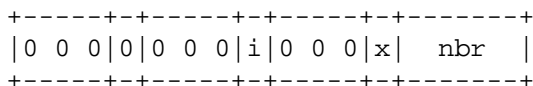
Register number for interpreted access mode (bit 12 = 1):



The 16bit register number is used to build the appropriate MCR/MRC instruction.

ARM940T, ARM946E, ARM966E:

The CP15 registers are directly accessed via JTAG.

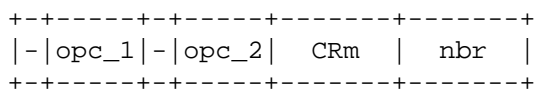


The bit "i" selects the instruction cache (scan chain bit 32), the bit "x" extends access to register 6 (scan chain bit 37).

```
WCP15 0x0005      0x00000000F data region 0/1 full access
WCP15 0x0105      0x00000000F inst region 0/1 full access
WCP15 0x0001      0x0000107D  enable protection and caches
```

ARM926E:

The 16bit register number contains the fields of the appropriate MCR/MRC instruction that would be used to access the CP15 register.



Normally opc_1, opc_2 and CRm are zero and therefore you can simply enter the CP15 register number.

TI925T:

The CP15 registers are directly accessed via JTAG.

The following table shows the numbers used to access the CP15 registers and functions.

- 0 (or 0x30) : ID
- 1 (or 0x31) : Control
- 2 (or 0x32) : Translation table base
- 3 (or 0x33) : Domain access control
- 5 (or 0x35) : Fault status
- 6 (or 0x36) : Fault address
- 8 (or 0x38) : Cache information
- 13 (or 0x3d) : Process ID

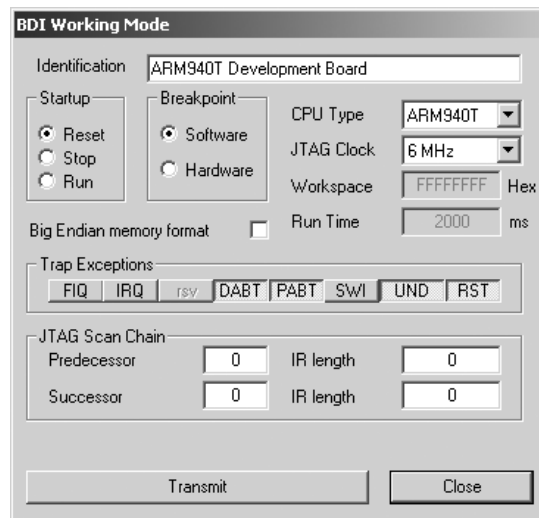
- 0x10 : TI925T Status
- 0x11 : TI925T Configuration
- 0x12 : TI925T I-max
- 0x13 : TI925T I-min
- 0x14 : TI925T Thread ID

- 0x18 : Flush I+D TLB
- 0x19 : Flush I TLB
- 0x1a : Flush I TLB entry
- 0x1b : Flush D TLB
- 0x1c : Flush D TLB entry

- 0x20 : Flush I cache
- 0x22 : Flush I cache entry
- 0x23 : Flush D cache
- 0x24 : Flush D cache entry address
- 0x25 : Clean D cache entry address
- 0x26 : Clean + Flush D cache entry address
- 0x27 : Flush D cache entry index
- 0x28 : Clean D cache entry index
- 0x29 : Clean + Flush D cache entry index
- 0x2a : Clean D cache
- 0x2b : Drain Write buffer

- 0x37 : I cache TLB Lock-Down
- 0x3a : D cache TLB Lock-Down

4 BDI working modes



dialog box «BDI Working Mode»

With this dialog box you can define how the BDI interacts with the target system.

Identification	Enter a text to identify this setup. This text can be read by the debugger with the appropriate Command.
Startup	Startup mode defines how the BDI interacts with the target processor after reset or power up. The options RESET, STOP or RUN can be selected.
Breakpoint	Breakpoint mode defines how instruction breakpoints are implemented. When Software is selected (default), instruction breakpoints are set as requested by the debugger (Soft or Hard). When Hardware is selected, the BDI uses always hardware breakpoints. Select Hardware and do not catch vectors when debugging code stored in ROM. Then the 2 hardware breakpoints of the ICEBreaker module can be used by the user. Otherwise only one is available, the other is used for software breakpoints.
CPU Type	Select the CPU type of the target system.
Workspace	If a workspace is defined, the BDI uses a faster download mode via the ARM's Debugger Communications Channel (DCC). The workspace is used for a short code sequence that reads from the DDC and writes to memory. There must be at least 32 bytes of RAM available for this code. There is no handshake between the BDI and the code consuming the data transferred via DCC. If the helper code on the target executes to slow, this download mode may fail and you have to disable it. A value of 0xFFFFFFFF disables the workspace.
Run Time	When startup mode STOP is selected, this option allows to set the run time after reset in milliseconds until the target CPU is stopped. Values from 100 (0.1 sec) till 32000 (32 sec) are accepted.

Trap Exceptions	<p>ARM9: Select the exceptions that should lead to debug mode entry instead of entering the normal exception handler. The IceBreaker's vector catch register is used for this.</p> <p>ARM7: Select the exceptions for which the BDI should install a default handler. The default handler is simply a software breakpoint. Catching exceptions is only possible if the memory at address 0x00000000 to 0x0000001F is writable.</p>
Big Endian...	Check this switch if the target memory uses Big Endian format.
JTAG Clock	This option allows to select the used JTAG clock rate (adaptive needs a special cable from Abatron, please ask for it).
JTAG Scan Chain	The BDI can also handle systems with multiple devices connected to the JTAG scan chain. In order to put the other devices into BYPASS mode and to count for the additional bypass registers, the BDI needs some information about the scan chain layout. Enter the number and total instruction register (IR) length of the devices present before the ARM chip (Predecessor). Enter the appropriate information also for the devices following the ARM chip (Successor).
Transmit	Click on this button to send the initialization list and the working mode to the BDI. This is normally the last step done before the BDI can be used with the debugging system.

4.1 Startup Mode

Startup mode defines how the BDI interacts with the target system after a reset or power up sequence.

4.1.1 Startup mode RESET

In this mode no ROM is required on the target system. The necessary initialization is done by the BDI with the programmed init list. The following steps are executed by the BDI after system reset or system power up:

- RESET is activated on the target system.
- RESET is deactivated and the target is forced into debug mode.
- The BDI works through the initialization list and writes to the corresponding addresses.

The RESET mode is the standard working mode. Other modes are used in special cases (i.e. applications in ROM, special requirements on the reset sequence...).

4.1.2 Startup Mode STOP

In this mode the initialization code is in a ROM on the target system. The code in this ROM handles base initialization. At the end of the code, the initialization program enters an endless loop until it is interrupted by the BDI. This mode is intended for special requirements on the reset sequence (e.g. loading a RAM based programmable logic device).

In this mode the following steps are executed by the BDI after system reset or power up:

- RESET is activated on the target system.
- RESET is deactivated and the target starts executing application code.
- After a delay of RUNTIME seconds, the target is forced into debug mode.
- The BDI works through the initialization list and writes the corresponding addresses.

4.1.3 Startup mode RUN

This mode is used to debug applications which are already stored in ROM. The application is started normally and is stopped when the debugger is started.

In this mode, the following steps are executed by the BDI after system reset or power up:

- RESET is activated on the target system.
- RESET is deactivated and the target starts executing application code.
- The application runs until it is stopped by the debugger.

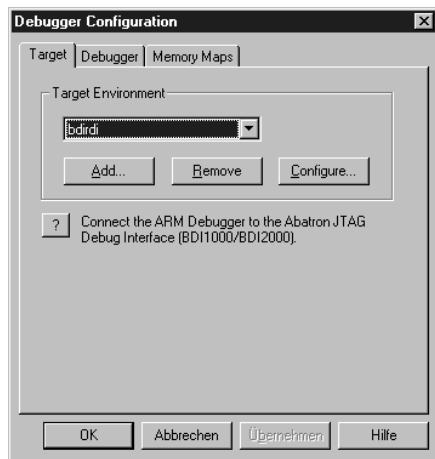
5 Working with RDI Debuggers

5.1 ADW/AXD from ARM Ltd.

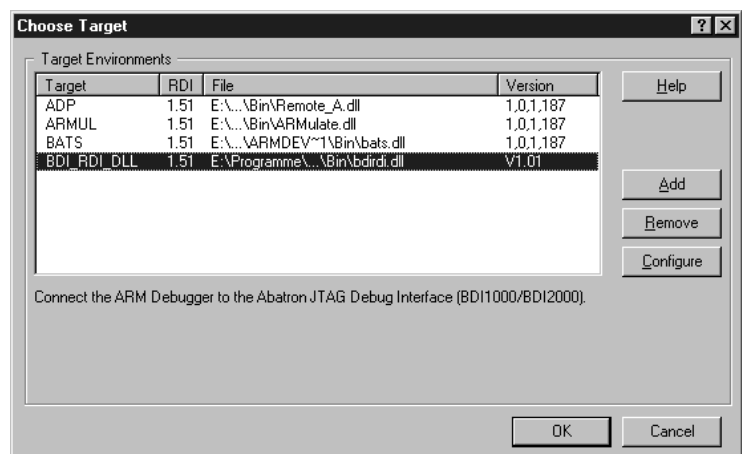
5.1.1 Configuration

In order work with ADW/AXD from ARM Ltd. copy the RDI interface DLL (bdirdi.dll) to the \bin subdirectory of your ARM Software Development Toolkit directory.

Start the ARM debugger and select "Options >> Configure Debugger..." / "Options >> Configure Target...". This opens the "Debugger Configuration" / "Choose Target" dialog box. Add BDIRDIT to the list of "Target Environment".

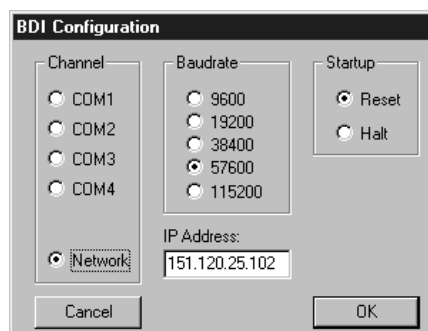


ADW



AXD

To setup the communication parameters, press button "Configure...". This opens the "BDI Communication Setup" dialog box. Enter the appropriate communication parameters.



The Startup mode defines how the BDI interacts with the target when the debugger starts. If Reset is selected (default), the BDI forces a hardware reset of the target when the debugger attaches. The Halt mode is useful when you would like to connect to a running target. The BDI simply stops the target when the debugger attaches. This way you can investigate the current status of the target.

5.1.2 Implementation notes

Interactive input of "Direct commands" is not supported, but download to flash is possible with the appropriate command files in the working directory. The execution of the command files can be observed in the RDI Log window. See also chapter "BDI Direct Commands".

BY default for ARM7 targets, the BDI Semihosting implementation uses a software breakpoint. Therefore Semihosting is only supported if breakpoint mode is "Software" and the SWI (semihosting) vector is writable. In cases where the vector table is in ROM, you can force the BDI to use a hardware breakpoint to support Semihosting via a special init list entry (see chapter 3 Init List).

For ARM9 targets the hardware vector catch register is used and therefore Semihosting works also if the vector table is in ROM

For ARM9 targets, the individual vector catch feature of ADW/AXD is supported and uses the ARM9 hardware vector catch register. In this case, do not check the "Catch unhandled exception" switch in the BDI Mode dialog box. Use the debugger's interface to define which vectors to catch.

5.2 BDI Direct Commands

For special functions (mainly for flash programming) the BDI supports so called «Direct Commands». This commands can be entered in a command file (e.g. PRELOAD.CMD) or if supported directly executed in the debugger's Command Line Window. This Direct Commands are not interpreted by the debugger but directly sent to the BDI. After processing the command the result is displayed in the debugger's Command Line Window.

Direct Commands are ASCII - Strings with the following structure:

<Object>.<Action> [<ParName>=<ParValue>]...

Example:

```
flash.erase addr=0x02800000
```

All names are case insensitive. Parameter values are numbers or strings. Numeric parameters can be entered as decimal (e.g. 700) or as hexadecimal (0x80000) values.

Note:

If the used debugger has built-in flash programming capability, then uses this feature to program flash. Downloading to flash via the BDI Direct Commands should only be used if the debugger has no own flash programming functions.

5.2.1 Target.Reset

This direct command executes a real physical reset of the target system.

5.2.2 Flash.Setup

In order to support loading into flash memory, the BDI needs some information about the used flash devices. Before any other flash related command can be used, this direct command must be executed.

Syntax:

```
flash.setup type=am29f size=0x80000 bus=32 workspace=0x1000
```

type	This parameter defines the type of flash used. It is used to select the correct programming algorithm. The following flash types are supported: AM29F, AM29BX8, AM29BX16, I28BX8, I28BX16, AT49, AT49X8, AT49X16 STRATAX8, STRATAX16, MIRROR, MORRORX8, MIRRORX16, I28BX32 AM29DX16, AM29DX32, CFM32, CFM16, LPC2000, STA2051, ADUC7000 ST30F, AT91SAM7S
size	The size of one flash chip in bytes (e.g. AM29F010 = 0x20000). This value is used to calculate the starting address of the current flash memory bank.
bus	The width of the memory bus that leads to the flash chips. Do not enter the width of the flash chip itself. The parameter TYPE carries the information about the number of data lines connected to one flash chip. For example, enter 16 if you are using two AM29F010 to build a 16bit flash memory bank.
workspace	If a workspace is defined, the BDI uses a faster programming algorithm that run out of RAM on the target system. Otherwise, the algorithm is processed within the BDI. The workspace is used for a 1kByte data buffer and to store the algorithm code. There must be at least 2kBytes of RAM available for this purpose.

MAC7100 internal flash (CFM32, CFM16):

To erase and program the MAC7100 Program Flash Module (CFM32) you have to access it via the programming interface address (0xFC100000). This programming interface address has to be used for erase and program commands. Before you can erase/program the Program or Data Flash Module, the CFM Clock Divider needs to be setup via an init list entry. Check the MAC7100 user's manual about how to setup the CFMCLKD. Keep in mind that the input frequency for the flash module is the IP clock with a frequency of 1/2 fsys. If for example the system clock is 8 MHz, the clock input to the flash is 4MHz and the correct value for CFMCKLD is 19 (0x13)..

```
WM8 0xFC0F0002 0x13 ;CFMCLKD: set clock divider for 8.0 MHz system clock
```

Syntax:

```
flash.setup type=cfm32 workspace=0x40000000
```

type	This parameter defines the type of flash used. Enter CFM32 when programming the Program flash. For the Data flash use CFM16.
workspace	If a workspace is defined, the BDI uses a faster programming algorithm that run out of RAM on the target system. Otherwise, the algorithm is processed within the BDI. The workspace is used for a to store the algorithm code. There must be at least 256 Bytes of RAM available for this purpose.

```
;Use internal SRAM for workspace
flash.setup type=cfm32 workspace=0x40000000
```

Philips LPC2000 internal flash:

The LPC2000 (LPC2xxx) internal flash is programmed using the LPC2000 built-in flash programming driver via the so called IAP Commands. Details about the IAP commands you find in the LPC2000 user's manual. This driver needs the current System Clock Frequency (CCLK) in KHz. This frequency has to be provided via the clock parameter. The BDI needs also a workspace of 2k bytes in the internal SRAM. It is used to store the data to program and to create a context from which the flash drivers can be called.

Syntax:

```
flash.setup type=lpc2000 size=0x20000 workspace=0x40001000 clock=14745
```

type	This parameter defines the type of flash used.
size	This parameter defines the size of the flash in bytes
workspace	A workspace in the internal SRAM is necessary for to store the data to program and to create a context from which the flash drivers can be called
clock	Enter the current System Clock Frequency (CCLK) in KHz.

Example how-to erase and program LPC2xxx 126k device (Ashling EVBA7):

```
flash.setup type=lpc2000 size=0x20000 workspace=0x40001000 clock=14745
flash.erase addr=0x7fff
flash.load addr=0x00000000 size=0x1e000
```

Example how-to erase and program LPC2xxx 256k device (Keil MCB2100)

```
flash.setup type=lpc2000 size=0x40000 workspace=0x40001000 clock=12000
flash.erase addr=0x1ffff
flash.load addr=0x00000000 size=0x3e000
```

Atmel AT91SAM7S internal flash:

The BDI supports programming of the Atmel AT91SAM7S internal flash. Before using any flash function it is important that the MC_FMR register is programmed with the correct values for FMCN and FWS. This can be done via the initialization list.

Syntax:

```
flash.setup type=at91sam7s size=0x10000
```

type	This parameter defines the type of flash used.
size	This parameter defines the size of the flash in bytes

Example how-to erase and program AT91SAM7S 64K device (AT91SAM7S-EK)

```
flash.setup type=at91sam7s size=0x10000
flash.erase addr=0x100000 mode=chip
flash.load addr=0x00000000 size=0x10000
```

5.2.3 Flash.Erase

This command allows to erase one flash sector, block or chip.

Syntax:

```
flash.erase addr=0x02800000 mode=chip
```

addr The start address of the flash sector to erase.

mode This parameter defines the erase mode. The following modes are supported: CHIP, BLOCK and SECTOR (default is sector erase)

MAC7100 internal flash (CFM32, CFM16):

This command allows to erase one flash page (4k/1k) or the complete flash (mass erase).

Syntax:

```
flash.erase addr=0xFC100000 mode=block
```

addr The start address of the flash page/module to erase.

mode This parameter defines the erase mode. The following modes are supported: BLOCK and SECTOR (default is sector (4k/1k page) erase)

```
;mass erase the whole MAC7100 flash
flash.setup type=cfm32 workspace=0x40000000
flash.erase addr=0xFC101000 mode=block

;Erase 4k program page at 0xFC101000 (0xFC101000..0xFC101FFF)
flash.setup type=cfm32 workspace=0x40000000
flash.erase addr=0xFC101000

;Erase 1k data page at 0xFE000000 (0xFE000000..0xFE0003FF)
flash.setup type=cfm16 workspace=0x40000000
flash.erase addr=0xFE000000
```

STA2051/ STR710F Internal Flash:

For the STA2051 / STR710F internal flash, the BDI assumes the following structure of the address.

14 bit reserved	2 bit bank 1	8 bit reserved	8 bit bank 0
--------------------	-----------------	-------------------	-----------------

Select the sectors to erase by setting the appropriate bit in the bank0 or bank1 field. You can only set bits in one bank at the same time. It is not possible to erase both banks in one step.

```
flash.erase addr=0x00000080 ;erase sector B0F7
flash.erase addr=0x000000FF ;erase all sectors of bank 0
flash.erase addr=0x00030000 ;erase all sectors of bank 1
```

ST30F7xx Internal Flash:

The ST30F7xx flash is handled like the STA2051 flash. The only difference is, that there exists only flash bank 0 but with 12 sectors.

```
flash.erase addr=0x00000FFF ;erase all sectors of bank 0
```

LPC2000 Internal Flash:

The erase parameter has a different meaning. It is not an address but a bit map of the sectors to erase (bit0 = erase sector 0, bit1 = erase ...). Following some examples:

```
flash.erase addr=0x000000F0 ;erase sector 4...7
flash.erase addr=0x00007FFF ;erase sector 0...14
flash.erase addr=0x00000002 ;erase only sector 1
```

Atmel AT91SAM7S internal flash:

The BDI supports erasing a page (sector) or the complete flash memory. Default is page erase:

```
flash.erase addr=0x100000 mode=chip ;erase the whole flash
flash.erase addr=0x100000 ;erase only one page
```

5.2.4 Flash.Load

This command enables loading to flash memory. If the address of a data block is within the given flash range, the BDI automatically uses the appropriate programming algorithm. This command must be executed before downloading is started.

Syntax:

```
flash.load addr=0x02800000 size=0x200000
addr          The start address of the flash memory
size         The size of the flash memory
```

Note: For LPC2000, programming will only succeed if during the download the addresses do continuously increase. Programming will fail in cases where data is written to a flash page N, then to a different page M and then again to page N. The BDI buffers the data for one page until data arrives for a different page or flash.idle is executed.

5.2.5 Flash.Idle

This command disables loading to flash memory.

Syntax:

```
flash.idle
```

Note: For LPC2000 it is necessary that after the download flash.idle is executed. This will flush the data buffers and program the remaining data stored in the BDI to the flash.

5.3 Download to Flash Memory

The BDI supports download and debugging of code that runs out of flash memory. To automate the process of downloading to flash memory, the BDI looks for two command files in the working directory.

PRELOAD.CMD This command file is executed just before download begins

POSTLOAD.CMD This command file is executed after download is terminated.

Following is an example used to download into the flash memory of the PID7T board (socket U12 with a AMD flash Am29F010).

PRELOAD.CMD:

```

;Reset target
target.reset
;
;Define used flash memory: AM29F010
flash.setup type=am29f size=0x20000 bus=8 workspace=0x00001000
;
;Erase sector 0 to 7 of flash memory bank
flash.erase addr=0x04000000
flash.erase addr=0x04004000
flash.erase addr=0x04004000
flash.erase addr=0x04008000
flash.erase addr=0x0400C000
flash.erase addr=0x04010000
flash.erase addr=0x04014000
flash.erase addr=0x04018000
flash.erase addr=0x0401C000
;
;Enable loading into flash
flash.load addr=0x04000000 size=0x200000

```

POSTLOAD.CMD:

```
flash.idle
```

Note:

Some Intel flash chips (e.g. 28F800C3, 28F160C3, 28F320C3) power-up with all blocks in locked state. In order to erase/program those flash chips, use the init list to unlock the appropriate blocks.

```

WM16  0xFFFF0000  0x0060      unlock block 0
WM16  0xFFFF0000  0x00D0
WM16  0xFFFF1000  0x0060      unlock block 1
WM16  0xFFFF1000  0x00D0
      . . . .
WM16  0xFFFF0000  0xFFFF      select read mode

```

Supported Flash Memories:

There are currently 3 standard flash algorithm supported. The AMD, Intel and Atmel AT49 algorithm. Almost all currently available flash memories can be programmed with one of this algorithm. The flash type selects the appropriate algorithm and gives additional information about the used flash.

- For 8bit only flash: AM29F (MIRROR), I28BX8, AT49
- For 8/16 bit flash in 8bit mode: AM29BX8 (MIRRORX8), I28BX8 (STRATAX8), AT49X8
- For 8/16 bit flash in 16bit mode: AM29BX16 (MIRRORX16), I28BX16 (STRATAX16), AT49X16
- For 16bit only flash: AM29BX16, I28BX16, AT49X16
- For 16/32 bit flash in 16bit mode: AM29DX16
- For 16/32 bit flash in 32bit mode: AM29DX32
- For 32bit only flash: I28BX32

The AMD and AT49 algorithm are almost the same. The only difference is, that the AT49 algorithm does not check for the AMD status bit 5 (Exceeded Timing Limits).

Only the AMD and AT49 algorithm support chip erase. Block erase is only supported with the AT49 algorithm. If the algorithm does not support the selected mode, sector erase is performed. If the chip does not support the selected mode, erasing will fail. The erase command sequence is different only in the 6th write cycle. Depending on the selected mode, the following data is written in this cycle (see also flash data sheets): 0x10 for chip erase, 0x30 for sector erase, 0x50 for block erase.

To speed up programming of Intel Strata Flash and AMD MirrorBit Flash, an additional algorithm is implemented that makes use of the write buffer. This algorithm needs a workspace, otherwise the standard Intel/AMD algorithm is used.

The following table shows some examples:

Flash	x 8	x 16	x 32	Chipsize
Am29F010	AM29F	-	-	0x020000
Am29F800B	AM29BX8	AM29BX16	-	0x100000
Am29DL323C	AM29BX8	AM29BX16	-	0x400000
Am29PDL128G	-	AM29DX16	AM29DX32	0x01000000
Intel 28F032B3	I28BX8	-	-	0x400000
Intel 28F640J3A	STRATAX8	STRATAX16	-	0x800000
Intel 28F320C3	-	I28BX16	-	0x400000
AT49BV040	AT49	-	-	0x080000
AT49BV1614	AT49X8	AT49X16	-	0x200000
M58BW016BT	-	-	I28BX32	0x200000
SST39VF160	-	AT49X16	-	0x200000
Am29LV320M	MIRRORX8	MIRRORX16	-	0x400000

6 Telnet Interface

A Telnet server is integrated within the BDI that can be accessed when the BDI is connected via ethernet to the host. It may help to investigate problems and allows access to target resources that can not directly be accessed by the debugger.

The following commands are available:

```
"MD      [<address>] [<count>]  display target memory as word (32bit)",
"MDH    [<address>] [<count>]  display target memory as half word (16bit)",
"MDB    [<address>] [<count>]  display target memory as byte (8bit)",
"MM      <addr> <value> [<cnt>] modify word(s) (32bit) in target memory",
"MMH    <addr> <value> [<cnt>] modify half word(s) (16bit) in target memory",
"MMB    <addr> <value> [<cnt>] modify byte(s) (8bit) in target memory",
"MT      <addr> <count>        memory test",
"MC      [<address>] [<count>] calculates a checksum over a memory range",
"MV      verifies the last calculated checksum",
"RD      display general purpose registers",
"RDALL   display all ARM registers ",
"RDCP   <number>              display control processor 15 register",
"RDIB   [<number>]           display IceBreaker register",
"RM      <number> <value>     modify general purpose or user defined register",
"RMCP   <number> <value>     modify control processor 15 register",
"RMIB   <number> <value>     modify IceBreaker register",
"BOOT   reset the BDI",
"RESET  reset the target system",
"GO     [<pc>]               set PC and start target system",
"TI     [<pc>]               single step an instruction",
"HALT   force target to enter debug mode",
"BI     <addr> [<mask>]      set instruction breakpoint",
"CI     [<id>]               clear instruction breakpoint(s)",
"BD     [R|W] <addr> [<data>] set data watchpoint (32bit access)",
"BDH    [R|W] <addr> [<data>] set data watchpoint (16bit access)",
"BDB    [R|W] <addr> [<data>] set data watchpoint ( 8bit access)",
"CD     [<id>]               clear data watchpoint(s)",
"INFO   display information about the current state",
"DCMD   <direct command>    execute a BDI direct command (see manual)",
"SCAN   <nbr><len>[<...b2b1b0>] Access a JTAG scan chain, b0 is first scanned",
"       len : the number of bits 1..256",
"       bx  : a data byte, two hex digits",
"HELP   display command list",
"QUIT   terminate the Telnet session"
```

7 Specifications

Operating Voltage Limiting	2.5 ... 5.25VDC
Power Supply Current (max)	900mA@2.5V 700mA@3.3V 450mA@5.0V
RS232 Interface: Baud Rates	9'600,19'200, 38'400, 57'600,115'200
Data Bits	8
Parity Bits	none
Stop Bits	1
Network Interface	10 BASE-T
Serial Transfer Rate between BDI and Target	5.5 Mbit/s (BDM) 12 Mbit/s (JTAG)
Supported target voltage	1.8 ... 5 VDC
Operating Temperature	+ 5 °C ... +60 °C
Storage Temperature	-20 °C ... +65 °C
Relative Humidity (noncondensing)	<90 %rF
Size	160 x 85 x 35 mm
Weight (without cables)	280 g
Electromagnetic Compatibility (EMC)	EN 50081-2, EN 50082-2

Specifications subject to change without notice

8 Environmental notice



Disposal of the equipment must be carried out at a designated disposal site.

9 Declaration of Conformity (CE)

CE

Declaration of Conformity

This declaration is valid for the following product:

Type of device:	BDM/JTAG Interface
Product name:	BDI1000

The signing authorities state, that the above mentioned equipment meets the requirements for emission and immunity according to

EMC Directive 89/336/EEC

The evaluation procedure of conformity was assured according to the following standards:


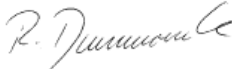
EN50081-2
EN50082-2

This declaration of conformity is based on the test report no. QNL-E079-05-9-a of Quinel, Zug, accredited according to EN 45001.

Manufacturer:

Abatron AG
Stöckenstrasse 4
CH-6221 Rickenbach

Authority:

 Max Vock Marketing Director	 Ruedi Dummermuth Technical Director
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Rickenbach, November 2, 1999

10 Warranty

ABATRON Switzerland warrants the physical diskette, cable, BDI1000 and physical documentation to be free of defects in materials and workmanship for a period of 24 months following the date of purchase when used under normal conditions.

In the event of notification within the warranty period of defects in material or workmanship, ABATRON will replace defective diskette, cable, BDI1000 or documentation. The remedy for breach of this warranty shall be limited to replacement and shall not encompass any other damages, including but not limited loss of profit, special, incidental, consequential, or other similar claims.

ABATRON Switzerland specifically disclaims all other warranties- expressed or implied, including but not limited to implied warranties of merchantability and fitness for particular purposes - with respect to defects in the diskette, cable, BDI1000 and documentation, and the program license granted herein, including without limitation the operation of the program with respect to any particular application, use, or purposes. In no event shall ABATRON be liable for any loss of profit or any other commercial damage, including but not limited to special, incidental, consequential, or other damages.

Failure in handling which leads to defects are not covered under this warranty. The warranty is void under any self-made repair operation except exchanging the fuse.

Appendices

A Troubleshooting

Problem

The firmware can not be loaded.

Possible reasons

- The BDI is not correctly connected with the target system (see chapter 2).
- The power supply of the target system is switched off or not in operating range (2.5 VDC ... 5 VDC) --> MODE LED is OFF or RED
- The built in fuse is damaged --> MODE LED is OFF
- The BDI is not correctly connected with the Host (see chapter 2).
- A wrong communication port (Com 1...Com 4) is selected.

Problem

No working with the target system (loading firmware is ok).

Possible reasons

- Wrong pin assignment (BDM/JTAG connector) of the target system (see chapter 2).
- Target system initialization is not correctly --> enter an appropriate target initialization list.
- An incorrect IP address was entered (BDI1000 configuration)
- BDM/JTAG signals from the target system are not correctly (short-circuit, break, ...).
- The target system is damaged.

Problem

Network processes do not function (loading the firmware was successful)

Possible reasons

- The BDI1000 is not connected or not correctly connected to the network (LAN cable or media converter)
- An incorrect IP address was entered (BDI1000 configuration)

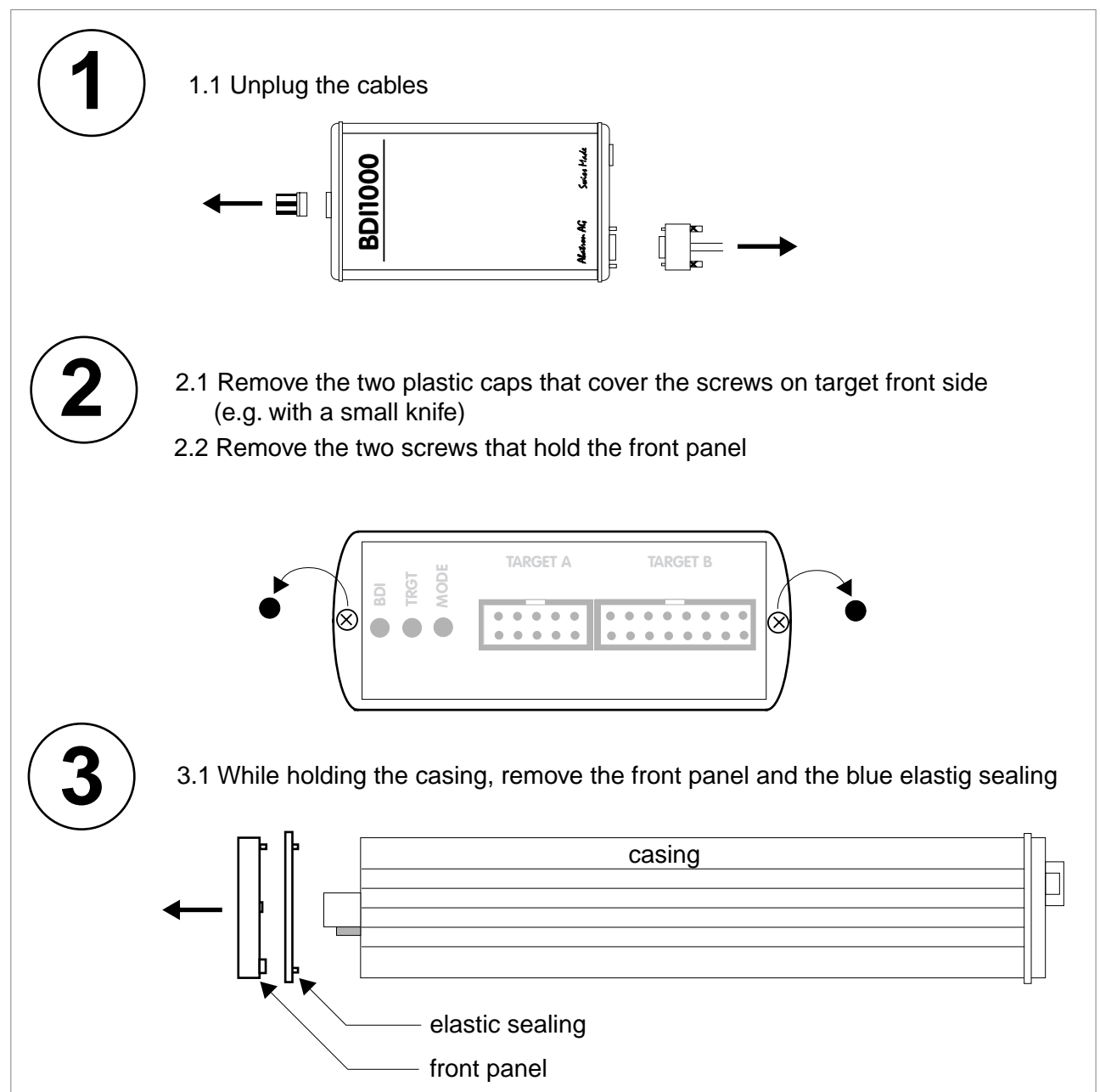
B Maintenance

The BDI needs no special maintenance. Clean the housing with a mild detergent only. Solvents such as gasoline may damage it.

If the BDI is connected correctly and it is still not responding, then the built in fuse might be damaged (in cases where the device was used with wrong supply voltage or wrong polarity). To exchange the fuse or to perform special initialization, please proceed according to the following steps:

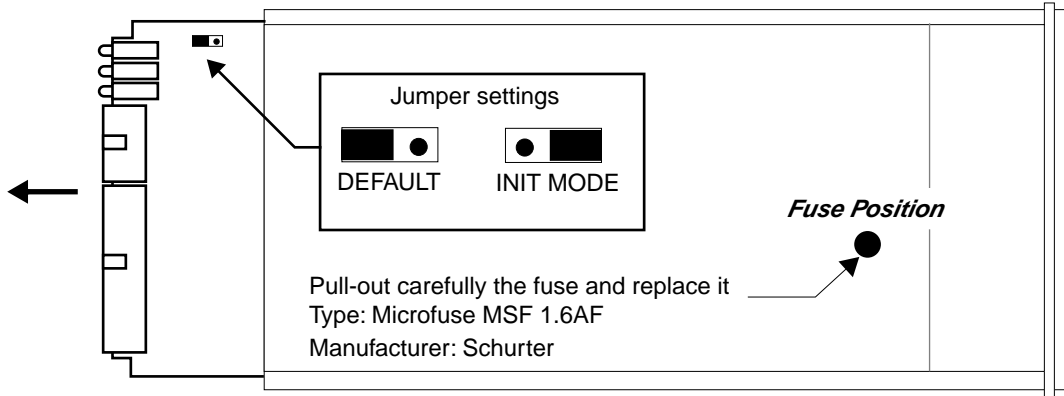


Observe precautions for handling (Electrostatic sensitive device)
Unplug the cables before opening the cover.
Use exact fuse replacement (Microfuse MSF 1.6 AF).



4

4.1 While holding the casing, slide carefully the print in position as shown in figure below

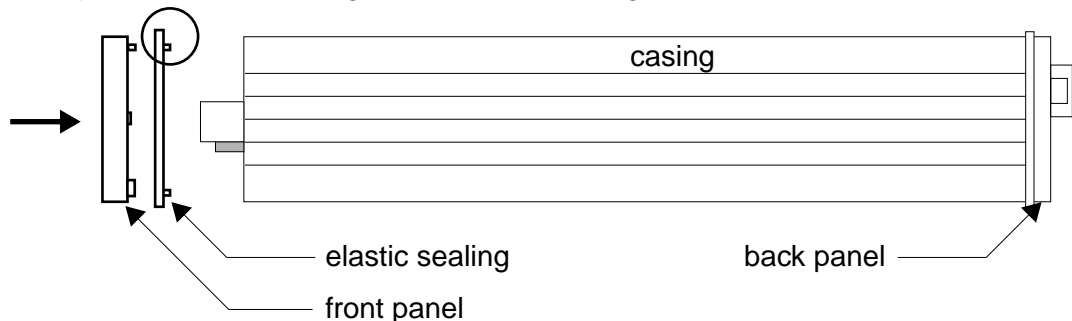


5

Reinstallation

5.1 Slide back carefully the print. Control that the LEDs align with the holes in the back panel.

5.2 Push carefully the front panel and the blue elastic sealing on the casing. Check that the LEDs align with the holes in the front panel and that the position of the sealing is as shown in the figure below.



5.3 Mount the screws (do not overtighten it)

5.4 Mount the two plastic caps that cover the screws

5.5 Plug the cables



Observe precautions for handling (Electrostatic sensitive device)
Unplug the cables before opening the cover.
Use exact fuse replacement (Microfuse MSF 1.6 AF).

C Trademarks

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