

Production Programming for HC12 internal Flash

1. Overview

The BDM interface called BDI1000 from Abatron offers the possibility to easy program the internal flash and EEPROM of Motorola HC12 devices during production. All information necessary to program the HC12 flash is stored within the flash of the BDI1000. You simply connect the BDI1000 to the HC12 BDM interface, power-up the system and wait until Success or Error is reported.

The following times has been measured from switching on power until Success was reported.

Device (ECLK = 8 MHz)	Erase/Program	Erase/Program/Verify
HC912B32 (32kB Flash)	4 sec	5 sec
HC912D60 (60kB Flash)	6 sec	9 sec
HC912DG128 (128kB Flash)	13 sec	19 sec
HC912DT128A (128kB Flash)	9 sec	15 sec
HC9S12DP256 (256kB Flash)	15 sec	26 sec
HC9S12DP256 (24MHz BDM Clk)	8 sec	14 sec

Note:

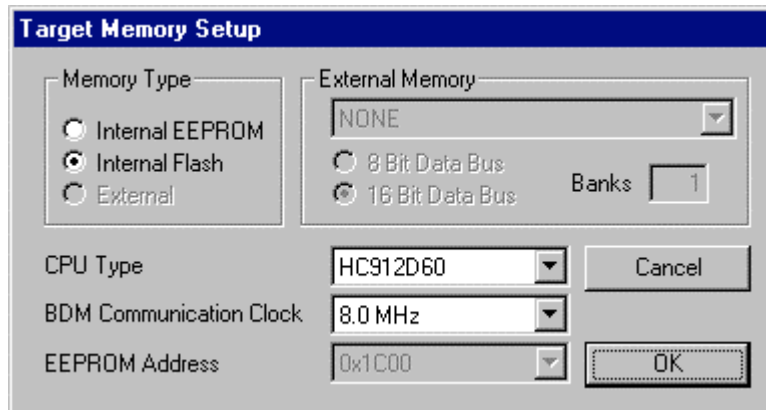
Automatic programming is not supported for devices with more than 256kB flash memory.

For more information about the BDI1000 visit us at www.abatron.ch

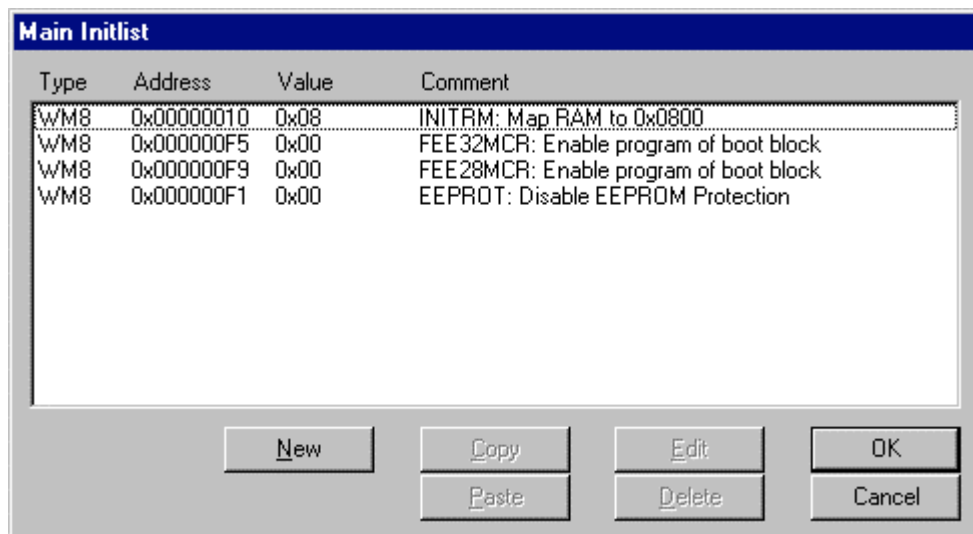
1.1. BDI1000 Setup

The configuration of the BDI1000 is made with an easy to use Windows program. This program, called bdiPro, also allows you to interactively program internal and external flash devices. You first can check your configuration parameters and then transmit this information to the BDI1000 for automatic programming. Following the steps to prepare the BDI1000 for HC912D60 automatic programming.

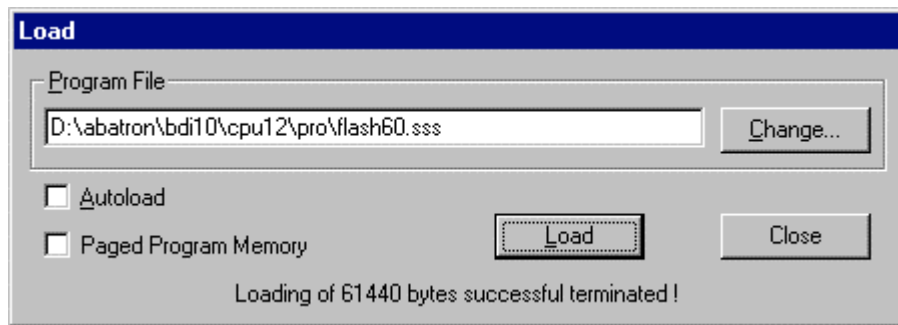
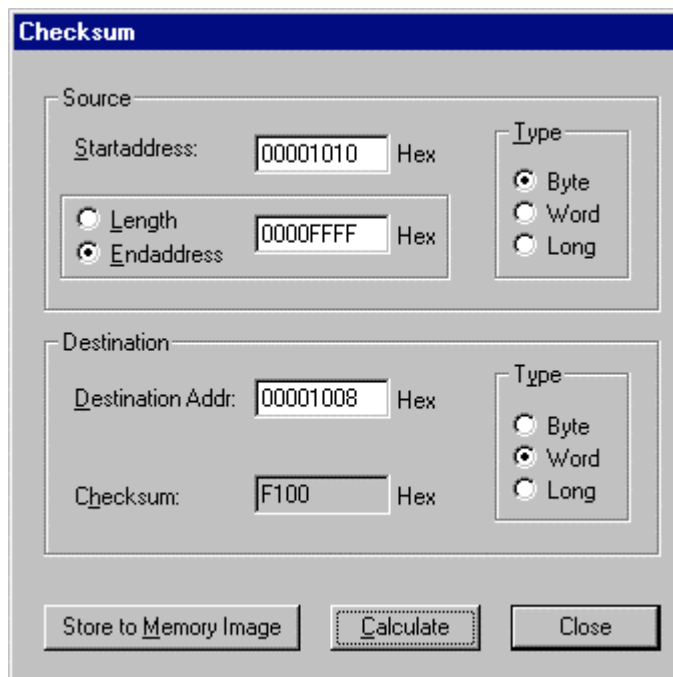
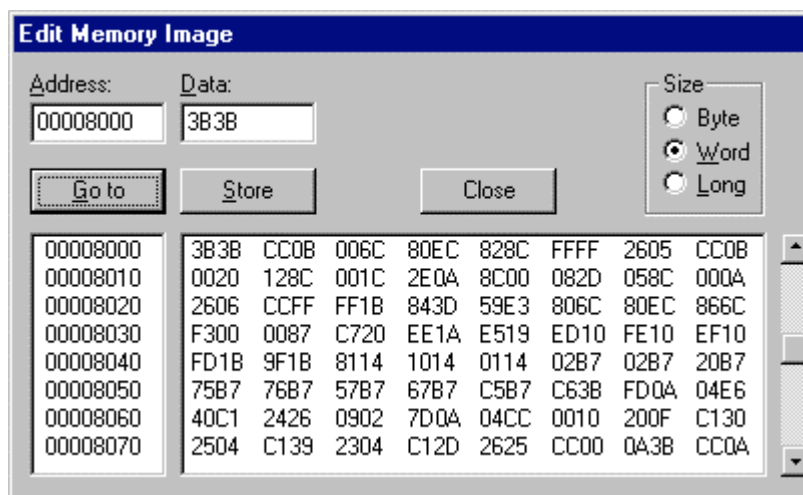
Select the device and memory type:



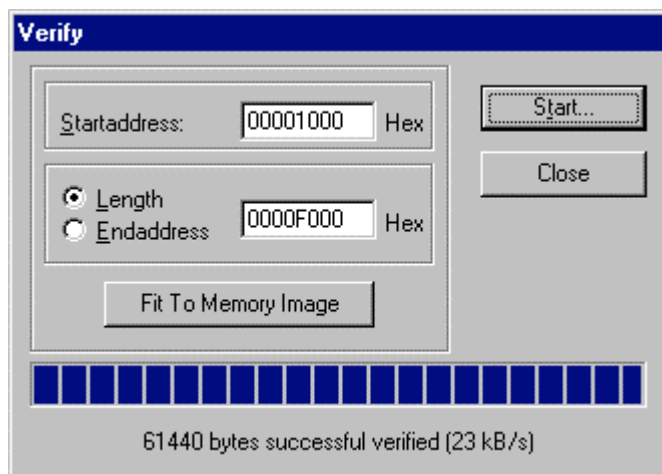
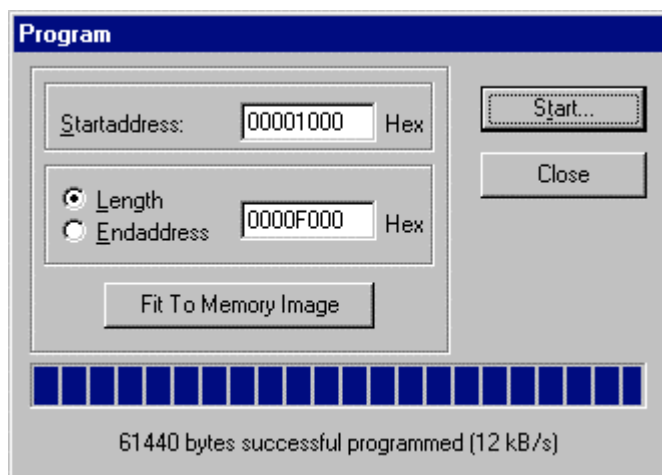
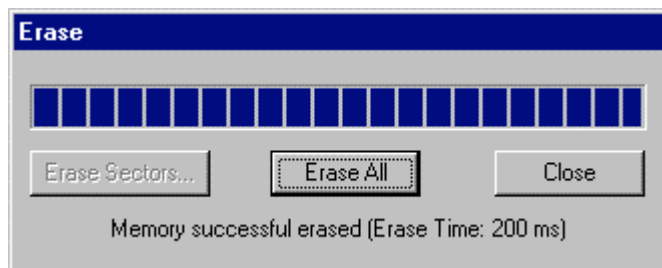
Prepare an initialization list to correctly setup the HC12 device:



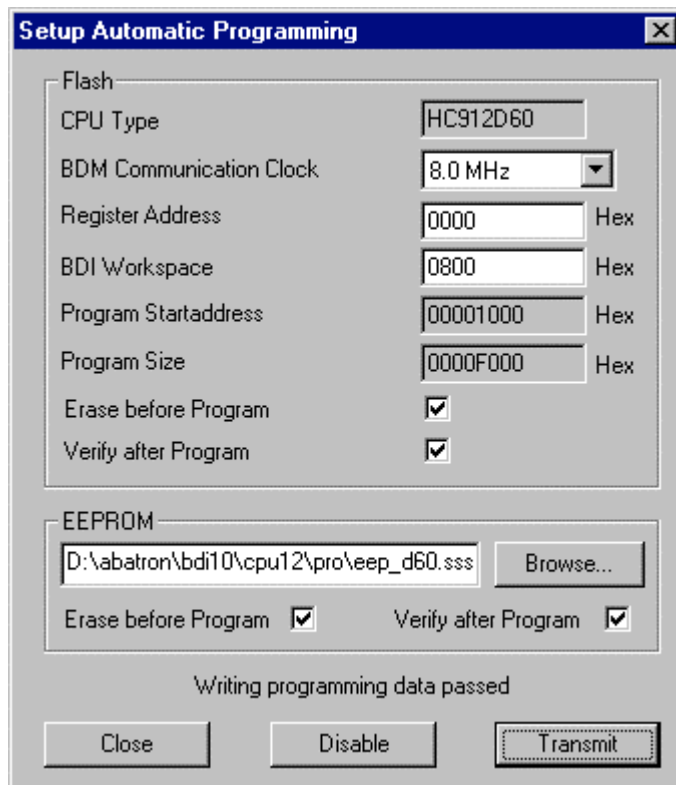
The last entry is only necessary if also the EEPROM will be programmed. Never enable the EEPROM because this may conflict with flash programming. The BDI automatically enables the EEPROM after programming the flash has finished.

Read in the data to program:**You may edit the program image or calculate checksums:**

In order to test the setup, you can interactively Erase, Program and Verify the Flash:



Now you can download the setup and the program image to the BDI1000:



If the EEPROM should also be programmed, enter the name of the S-Record file with the EEPROM data. Do not forget to disable EEPROM block protection with an entry in the init list. The BDI1000 is now ready for automatic programming.

1.2. Automatic Programming

After the programming data is stored within the flash of the BDI1000, the automatic programming sequence will be started every time the BDI1000 detects that the target is powered up. The BDI1000 itself should be powered all the times with an external power supply.

The following steps are executed after a target power-up is detected:

- The target is reseted
- The initialization list is processed
- If selected, the flash is erased
- The flash is programmed
- If selected, the flash data is verified (read back), else checksum is compared
- If selected, the EEPROM is erased
- If selected, the EEPROM is programmed
- If selected, the EEPROM data is verified (read back)

The programming state can be monitored in different ways:

- The red MODE LED signals the following states:

RED	automatic programming is running
OFF	programming terminated without error
TOGGLE	programming terminated with error

Note: The error case (5 Hz toggle rate) is only displayed for 10 seconds, then the LED goes off.

- Two TTL state pins:

S1	S0	Programming State
0	0	running (or Vcc Target < 2.5V)
0	1	success
1	0	error
1	1	start-up, idle

Note: The signals S1 / S2 are only valid, if the target is powered up (BDM pin 9 > 2.5V).

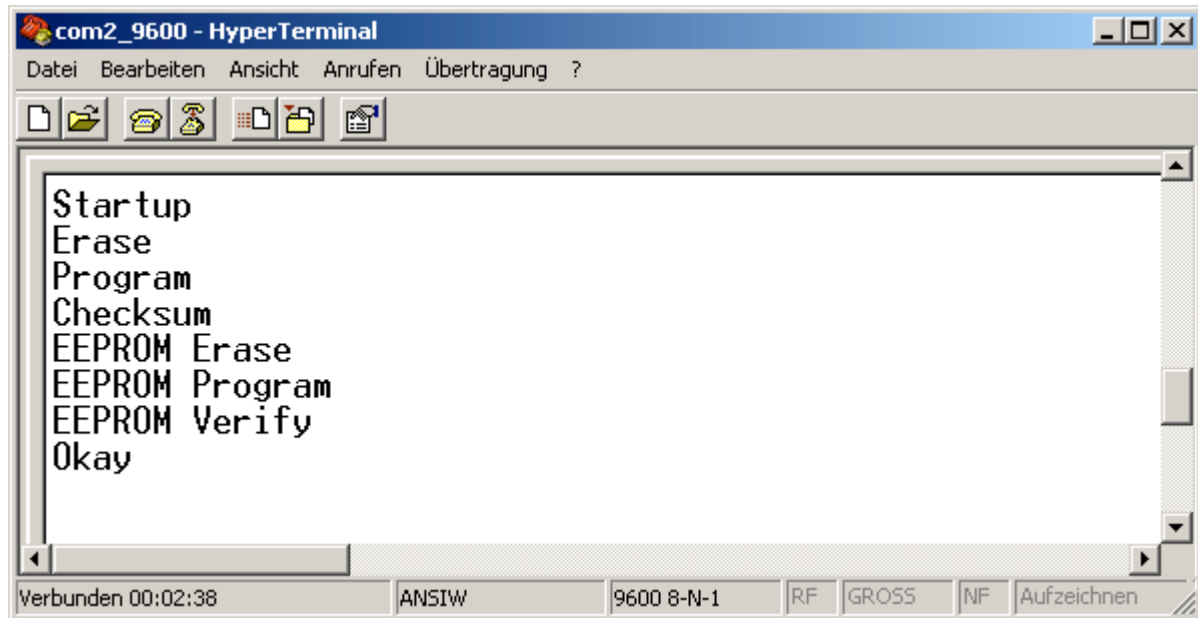
- Text output at the RS232 interface:

```

RS232 Direct - HyperTerminal
Datei Bearbeiten Ansicht Anruf Übertragung ?
Startup
Erase
Program
Verify
EEPROM Erase
EEPROM Program
EEPROM Verify
Okay
Verbunden 00:03:03 ANSI 9600 8-N-1 RF GROSS
  
```

With firmware version 1.09, a checksum compare of the flash data has been added. This checksum compare is executed if "Verify" is not selected for the flash memory. The checksum check is much faster than the "Verify" because the checksum is calculated with code that runs on the HC12 target.

The output in this case looks as follows:



```
com2_9600 - HyperTerminal
Datei Bearbeiten Ansicht Anrufen Übertragung ?
Startup
Erase
Program
Checksum
EEPROM Erase
EEPROM Program
EEPROM Verify
Okay
Verbunden 00:02:38 ANSIW 9600 8-N-1 RF GROSS NF Aufzeichnen
```

After programming, the checksum code is loaded into target SRAM. This code is then started and while it executes, the BDI itself calculates the sum over the data stored in its flash memory. After the code running on the target terminates, the two sums are compared. For a paged flash memory system, the sum is calculated and compared for every programmed page.

If "Verify" is selected, then every programmed byte is read back via the BDM interface and compared with the one stored in the BDI flash memory.

With the new checksum feature, there is no need for a full "Verify" but it is left there for compatibility.

1.3. How to speed-up programming on HCS12 devices

The time needed to program the internal flash of a HCS12 device depends heavily on the used BDM clock rate. By default, the BDM clock rate is $\frac{1}{2}$ of the connected crystal/oscillator frequency. For example if there is a 4MHz oscillator connected to the HCS12 device, BDM clock rate is only 2 MHz. This gives you very poor programming speed. Fortunately there is a way to speed-up the BDM clock rate by using the HCS12 internal PLL. For this, setup the PLL to generate the desired BUS frequency (e.g. 24MHz) and then switch SYSCLK clock source, BDM clock source and BDI communication speed with one special entry in the init list.

Following an example where BDM clock changes from 8MHz to 24MHz on a HC9S12DP256 system with a 16MHz oscillator. The complete setup you will find in "s256_pll.pro".

```

...
WM8      0x00000035  0x07  REFDV: Divide reference by 8
WM8      0x00000034  0x0B  SYNRR: Multiply by 12 => 48MHz System => 24MHz Bus
DELAY    100      Let PLL lock
WM8      0x81000039  0x80  CLKSEL: Set PLLSEL, set CLKSW=1, 24MHz BDM clock
          ||      ||      ||
          ||      ||      +-+ data for the CLKSEL registers
          +-+----- CLKSEL registers address
          +----- selects the BDI's BDM clock (1 = 24MHz), see below
          +----- marks this entry as BDM clock switch

```

BDI1000 clock rate table :

0 = ECLK	10 = 5.5 MHz	20 = 2.0 MHz
1 = 24 MHz	11 = 5.3 MHz	21 = 1.7 MHz
2 = 16 MHz	12 = 4.8 MHz	22 = 1.5 MHz
3 = 12 MHz	13 = 4.4 MHz	23 = 1.2 MHz
4 = 11 MHz	14 = 4.0 MHz	24 = 1.0 MHz
5 = 9.6 MHz	15 = 3.7 MHz	
6 = 8.0 MHz	16 = 3.0 MHz	
7 = 7.3 MHz	17 = 2.7 MHz	
8 = 6.8 MHz	18 = 2.4 MHz	
9 = 6.0 MHz	19 = 2.2 MHz	

Important note:

The changed system clock has almost no influence on the value used for the Flash Clock Divider register FCLKDIV. The reference clock for the calculation of FCLKDIV is the oscillator frequency. Carefully read the appropriate chapter about how to determine the FCLKDIV value in the HCS12 user's manual.

Remark:

Only BDI firmware version 1.08 or newer supports this BDM clock switch function.